<div align="center">REMARKS</div>

Claims 1-29 are pending.

<div align="center">Specification</div>

The specification is amended to include reference to element 740 of Figure 7.

The title is amended, in response to the Examiner's requirement for a new title.

<div align="center">102 Rejections</div>

The instant Office Action states that Claims 1-3, 11-15 and 23-24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Yates, Jr. et al. (U.S. Patent No. 6,397,379; hereinafter "Yates"). The Applicants have reviewed the cited reference and respectfully submit that the present invention as recited in Claims 1-3, 11-15 and 23-24 is not anticipated by Yates.

Independent Claim 1 recites a method that includes "registering a first address for a <u>native</u> instruction associated with said commit operation; and registering a second address used for recovering a <u>non-native</u> instruction associated with said commit operation" (emphases added). Independent Claim 14 recites a method that includes "<u>performing a rollback operation</u> to return to said commit point using a first address to locate a <u>native</u> instruction associated with said commit point; and <u>in conjunction with said rollback operation</u>, using a second address to recover a <u>non-native</u> instruction

associated with said commit point" (emphases added). Independent Claim 23 recites a method that includes "reading an address in a register, said address pointing to a <u>native</u> instruction having an indicator bit and a plurality of pointer bits, wherein <u>depending on the value of said indicator bit</u>, said pointer bits point <u>either</u> to an effective instruction pointer for a <u>non-native</u> instruction associated with said commit point <u>or</u> to information that can be used for recovering said effective instruction pointer" (emphases added).

For anticipation under 35 U.S.C. § 102, Yates must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. However, the fact that a certain characteristic may occur or be present in Yates is not sufficient to establish the inherency of that characteristic. To establish inherency, it must be clear from Yates that the missing descriptive matter is necessarily present and that it would be recognized by persons of ordinary skill.

Moreover, according to the Federal Circuit, "[a]nticipation requires the disclosure in a single prior art reference of each claim under consideration" (W.L. Gore & Assocs. v. Garlock Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983)). However, it is not sufficient that the reference recite all the claimed elements. As stated by the Federal Circuit, the prior art reference <u>must</u> disclose each element of the claimed invention "<u>arranged as in the claim</u>" (emphases added; Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)).

Applicants respectfully submit that, in light of the above requirements, Yates does not anticipate the present claimed invention recited in independent Claims 1, 14 and 23. The context switch of Yates only switches from one X86 (e.g., non-native) thread to another X86 (e.g., non-native) thread. Hence, the limitations of Claims 1, 14 and 23 cited above, which refer to both native and non-native instructions, are not "part of the context switching as described." Furthermore, because Yates only describes switching between two non-native threads, Applicants respectfully submit that the limitations of Claims 1, 14 and 23 cited above are not inherent in Yates.

Furthermore, with regard to independent Claim 14, Applicants respectfully submit that Yates does not show or suggest using a first address to locate a native instruction and using a second address to recover a non-native instruction, where these actions are performed in conjunction with a rollback operation. The portion of Yates cited in the instant Office Action appears to only describe that an X86-to-Tapestry (e.g., non-native to native) transition exception is vectored to an exception handler, which is described further starting at line 10 in column 34 of Yates. That discussion refers only to the EPC, which appears to be the native instruction pointer (see column 32, lines 38-39, of Yates). There appears to be no mention of a non-native instruction pointer.

In addition, with regard to independent Claim 23, Applicants respectfully submit that Yates does not show or suggest an indicator bit that is used as recited in the claim. That is, Claim 23 recites that one of two

actions can be taken, conditioned on the value of the indicator bit. However, Yates does not show or suggest such a condition, and in particular Yates does not show or suggest such a condition being applied to the recovery of a non-native instruction pointer.

In summary, Applicants respectfully submit that Yates does not show or suggest the limitations of independent Claims 1, 14 and 23, and that the rejection of these claims under 35 U.S.C. § 102(b) is traversed. Applicants also submit that the rejection of Claims 2-3, 11-13, 15 and 24 under 35 U.S.C. § 102(b) is traversed, as Claims 2-3, 11-13, 15 and 24 are dependent on Claim 1, 14 or 23 and recite additional limitations.

<div align="center">103 Rejections</div>

Claims 4-6 and 16-19

The instant Office Action states that Claims 4-6 and 16-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yates in view of Spix et al. (U.S. Patent No. 6,195,676; hereinafter "Spix"). The Applicants have reviewed the cited references and respectfully submit that the present invention as recited in Claims 4-6 and 16-19 is not shown or suggested by Yates and Spix, alone or in combination.

Claims 4-6 are dependent on independent Claim 1 and recite additional limitations, and Claims 16-19 are dependent on independent Claim 14 and recite additional limitations. Hence, by demonstrating that the cited references do not show or suggest the limitations of Claims 1 and 14, it

is also demonstrated that the cited references do not show or suggest the limitations of Claims 4-6 and 16-19.

As presented above, Applicants respectfully submit that Yates does not show or suggest the limitations of Claims 1 and 14. Applicants also submit that Spix does not overcome the shortcomings of Yates. Specifically, Applicants respectfully submit that Spix, alone or in combination with Yates, does not show or suggest a method that includes "registering a first address for a <u>native</u> instruction associated with said commit operation; and registering a second address used for recovering a <u>non-native</u> instruction associated with said commit operation" (emphases added) as recited in Claim 1, nor a method that includes "<u>performing a rollback operation</u> to return to said commit point using a first address to locate a <u>native</u> instruction associated with said commit point; and <u>in conjunction with said rollback operation</u>, using a second address to recover a <u>non-native</u> instruction associated with said commit point" (emphases added) as recited in Claim 14.

Therefore, Applicants respectfully submit that Claims 1 and 14 are allowable over the cited references. Accordingly, Applicants also submit that the rejection of Claims 4-6 and 16-19 under 35 U.S.C. § 103(a) is traversed, as Claims 4-6 and 16-19 are dependent on allowable base claims.

<u>Claims 8-10, 25 and 29</u>

The instant Office Action states that Claims 8-10, 25 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yates in view of Chung et al. (U.S. Patent No. 6,044,475; hereinafter "Chung"). The

Applicants have reviewed the cited references and respectfully submit that the present invention as recited in Claims 8-10, 25 and 29 is not shown or suggested by Yates and Chung, alone or in combination.

Claims 8-10 are dependent on independent Claim 1 and recite additional limitations, and Claims 25 and 29 are dependent on independent Claim 23 and recite additional limitations. Hence, by demonstrating that the cited references do not show or suggest the limitations of Claims 1 and 23, it is also demonstrated that the cited references do not show or suggest the limitations of Claims 8-10, 25 and 29.

As presented above, Applicants respectfully submit that Yates does not show or suggest the limitations of Claims 1 and 23. Applicants also submit that Chung does not overcome the shortcomings of Yates. Specifically, Applicants respectfully submit that Chung, alone or in combination with Yates, does not show or suggest a method that includes "registering a first address for a native instruction associated with said commit operation; and registering a second address used for recovering a non-native instruction associated with said commit operation" (emphases added) as recited in Claim 1, nor a method that includes "reading an address in a register, said address pointing to a native instruction having an indicator bit and a plurality of pointer bits, wherein depending on the value of said indicator bit, said pointer bits point either to an effective instruction pointer for a non-native instruction associated with said commit point or to information that can be used for recovering said effective instruction pointer" (emphases added) as recited in Claim 23.

Therefore, Applicants respectfully submit that Claims 1 and 23 are allowable over the cited references. Accordingly, Applicants also submit that the rejection of Claims 8-10, 25 and 29 under 35 U.S.C. § 103(a) is traversed, as Claims 8-10, 25 and 29 are dependent on allowable base claims.

Claims 7, 20-22 and 26-28

The instant Office Action states that Claims 7, 20-22 and 26-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yates in view of Spix and Chung. The Applicants have reviewed the cited references and respectfully submit that the present invention as recited in Claims 7, 20-22 and 26-28 is not shown or suggested by Yates, Spix and Chung, alone or in combination.

Claim 7 is dependent on independent Claim 1 and recites additional limitations, Claims 20-22 are dependent on independent Claim 14 and recite additional limitations, and Claims 26-28 are dependent on independent Claim 23 and recite additional limitations. Hence, by demonstrating that the cited references do not show or suggest the limitations of Claims 1, 14 and 23, it is also demonstrated that the cited references do not show or suggest the limitations of Claims 7, 20-22 and 26-28.

As presented above, Applicants respectfully submit that Yates and Spix, alone or in combination, do not show or suggest the limitations of Claims 1 and 14, and Yates and Chung, alone or in combination, do not show or suggest the limitations of Claims 1 and 23. Applicants also submit that

Chung does not overcome the shortcomings of Yates and Spix, and that Spix does not overcome the shortcomings of Yates and Chung. Specifically, Applicants respectfully submit that Yates, Spix and Chung, alone or in combination, do not show or suggest a method that includes "registering a first address for a native instruction associated with said commit operation; and registering a second address used for recovering a non-native instruction associated with said commit operation" (emphases added) as recited in Claim 1; nor a method that includes "performing a rollback operation to return to said commit point using a first address to locate a native instruction associated with said commit point; and in conjunction with said rollback operation, using a second address to recover a non-native instruction associated with said commit point" (emphases added) as recited in Claim 14; nor a method that includes "reading an address in a register, said address pointing to a native instruction having an indicator bit and a plurality of pointer bits, wherein depending on the value of said indicator bit, said pointer bits point either to an effective instruction pointer for a non-native instruction associated with said commit point or to information that can be used for recovering said effective instruction pointer" (emphases added) as recited in Claim 23.

Therefore, Applicants respectfully submit that Claims 1, 14 and 23 are allowable over the cited references. Accordingly, Applicants also submit that the rejection of Claims 7, 20-22 and 26-28 under 35 U.S.C. § 103(a) is traversed, as Claims 7, 20-22 and 26-28 are dependent on allowable base claims.
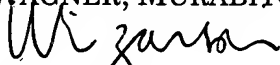
<u>Conclusions</u>

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-29 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these claims.

Applicants have reviewed the references cited but not relied upon, and did not find these references to show or suggest the present claimed invention: U.S. Patent Nos. 4,920,477, 5,057,837 and 6,401,216.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

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Respectfully submitted,

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